DECLARATION

I, Arata Iwasaki, of c/o SHIGA INTERNATIONAL PATENT OFFICE, Gran Tokyo South Tower, 1-9-2 Marunouchi, Chiyoda-ku, Tokyo, JAPAN, understand both English and Japanese, am the translator of the English document attached, and do hereby declare and state that the attached English document contains an accurate translation of the official certified copy of Japanese Patent Application No. 2004-184758 and that all statements made herein are true to the best of my knowledge.

Declared in Tokyo, Japan

This Tenth Day of April, 2009

.....Arata Iwasaki.....

Arata Iwasaki

DESCRIPTION

SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

TECHNICAL FIELD

[0001]

The present invention relates to a semiconductor device including a high dielectric constant insulating film and a method of fabricating the same, and more particularly to MOSFET (Metal Oxide Semiconductor Field Effect Transistor) accomplishing high performances and high reliability.

BACKGROUND ART

[0002]

In the development of a CMOS (Complementary MOS) device having a progressively miniaturized transistor, a reduction in a drive current due to depletion of a poly-silicon (poly-Si) electrode and an increase in a gate leak current due to a reduction in a thickness of a gate insulating film are problematic. Hence, combined technology for avoiding depletion of an electrode by use of a metal gate electrode, and further for reducing a gate leak current by use of, as a gate insulating film, a high dielectric constant material to thereby physically thicken a gate insulating film has been considered.

[0003]

As a material to be used as a metal gate electrode, pure metal, metal nitride, and silicide are considered. Whichever material is used, it is required that a threshold voltage (Vth) of n-type and p-type MOSFETs can be set to be an appropriate voltage.

[0004]

In order to accomplish a threshold voltage (Vth) equal to or smaller than ±0.5 eV in a CMOS transistor, it would be necessary to use a gate electrode made of a material having a work function equal to or smaller than a mid-gap (4.6 eV) of silicon (Si) or preferably equal to or smaller than 4.4 eV in n-type MOSFET, or a material having a work function equal to or greater than a mid-gap (4.6 eV) of silicon (Si) or preferably equal to or greater than 4.8 eV in p-type MOSFET.

[0005]

To this end, there has been suggested a method of controlling a threshold voltage (Vth) of a transistor by using gate electrodes of metals or alloys having different work functions as electrodes of n-type and p-type MOSFETs, respectively, which are generally called "dual metal gate".

[0006]

For instance, the non-patent reference 1 discloses that tantalum (Ta) and ruthenium (Ru) formed on silicon dioxide (SiO2) have work functions of 4.15 eV and 4.95 eV, respectively, and it is possible to modulate a work function by 0.8 eV between gate electrodes composed of these two metals.

[0007]

A silicide electrode comprising a poly-Si electrode fully silicided with nickel (Ni), hafnium (Hi) or tungsten (W) recently draws attention. For instance, the non-patent references 2 and 3 disclose technology as shown in FIG. 2 (b) in which the gate insulating film is composed of silicon dioxide (SiO2). Additionally, the gate electrode is composed of a nickel silicide (NiSi) electrode (P doped NiSi, B doped NiSi) formed by fully siliciding a poly-silicon electrode into which an impurity such as phosphorus (P) or boron (B) is implanted, thereby modulating a work function of the electrode by 0.5 eV. The technology is characterized in that it is possible to silicide a

poly-silicon electrode after impurities included in source/drain diffusion regions in CMOS are annealed for activation, ensuring that the process matches well with a conventional CMOS process.

[0008]

The non-patent references 2 and 3 disclose that NiSi and $NiSi_2$ made as gate electrodes have work functions of about 4.6 eV and about 4.45 eV, respectively, if a gate insulating film is composed of SiON.

[0009]

As shown in FIG. 2 (c), the non-patent document 1 also discloses technology in which tungsten (W) and tungsten silicide are separately used as gate electrodes or the composition of tungsten silicide is varied in order to control threshold voltages (Vth) of the n-type and p-type MOSFETs fabricated by a gate substitution process with use of tungsten (W) and tungsten silicide as gate electrodes. Specifically, a tungsten film or a tungsten silicide film is formed entirely on a substrate. Then, a silicon (Si) film and a tungsten film are formed on the tungsten film and the tungsten silicide film, respectively. Thereafter, the silicon film disposed on the tungsten film in the p-type MOSFET region or the tungsten film disposed on the tungsten silicide film in the n-type MOSFET region are removed. Then, the tungsten film and the silicon film, or the tungsten silicide film and the tungsten film are caused to react with each other by annealing to thereby form the tungsten silicide electrode and the tungsten electrode in the n-type and p-type MOSFET regions, respectively. Alternatively, the composition of the tungsten silicide is varied to control a work function of the gate electrode.

[Patent reference 1] Japanese Unexamined Patent Application, First Publication No. 2003-258121

[Non-patent reference 1] International electron devices meeting technical

digest 2002, p. 359

[Non-patent reference 2] International electron devices meeting technical digest 2002, p. 247

[Non-patent reference 3] International electron devices meeting technical digest 2003, p. 315

DISCLOSURE OF THE INVENTION

Problems to be Solved by the Invention

[0010]

However, the aforementioned prior art has the following problems. In the dual metal gate process in which metals or alloys having work functions different from one another are used, it is necessary to carry out a step of etching a layer formed on a gate of either the p-type or n-type MOSFET for removal. Additionally, a gate insulating film is degraded in the etching step, resulting in deterioration in performances and reliability of a resultant device.

[0011]

In the process of modulating the threshold voltage (Vth) by use of the impurity-doped silicide electrode, it is not possible to control a work function of a gate electrode when a gate insulating film is composed of a high dielectric constant material, as will be explained later with a reference example 2.

[0012]

In the process of modulating a work function by composing the gate electrodes of NiSi and $NiSi_2$, respectively, the work function becomes smaller. Hence, it is difficult to apply the process to a p-type MOSFET. Furthermore, as explained in the later-mentioned embodiment 1, if a gate insulating film is comprised of a high dielectric

constant insulating film, a difference in a work function between the gate electrode and the gate insulating film is equal to or smaller than 0.1 eV, resulting in that the modulation effect is suppressed.

[0013]

The process for changing the composition of tungsten silicide to change a work function of a gate electrode has a problem that since tungsten silicide is formed at a relatively high temperature, specifically, at 500 degrees centigrade or higher, a silicide layer formed in source/drain diffusion regions would be highly resistive. Furthermore, since the composition ratio of tungsten silicide and a work function of a gate electrode are in linear relation with each other, even slight non-uniformity in the composition ratio (for instance, non-uniformity in a thickness of a tungsten or silicon film, and non-uniformity in in-plane profile of the same) would cause fluctuation in the work function, resulting in reduction in reproduction and uniformity of a device. Furthermore, when a tungsten film and a silicon film are caused to react with each other to make silicon-rich tungsten silicide, there might cause peeling in an interface between a gate insulating film and a gate electrode.

[0014]

In view of the above-mentioned problems in the prior art, it is an object of the present invention to provide a semiconductor device and a method of fabricating the same both of which are capable of solving the above-mentioned problems, and enhancing performances and reliability of a resultant semiconductor device.

Means for Solving the Problems

[0015]

In one aspect of the present invention, there is provided a semiconductor device

including a silicon substrate, a gate insulating film formed on the silicon substrate, and a gate electrode formed on the gate insulating film, in this order. The gate insulating film includes a high dielectric constant insulating film containing one of metal oxide, metal silicate and metal oxide or metal silicate containing nitrogen therein. The gate electrode contains silicide of metal M as a primary constituent, and has a region through which the gate electrode makes contact with the gate insulating film and which has a composition expressed as M_xSi_{1-X} ($0<X<1$), and X is greater than 0.5 ($X>0.5$) in the silicide contained in a gate electrode formed above a p-channel, and X is equal to or smaller than 0.5 ($X\leq 0.5$) in the silicide contained in a gate electrode formed above an n-channel.

[0016]

In the semiconductor device, preferably, said high dielectric constant insulating film contains one of Hf and Zr. Alternatively, a layer containing one of Hf and Zr is included between said high dielectric constant insulating film and said gate electrode. Alternatively, said high dielectric constant insulating film has a multi-layered structure including one of a silicon oxide film and a silicon nitride film, and one of a Hf-containing layer and a Zr-containing layer. Alternatively, said high dielectric constant insulating film contains HfSiON. Alternatively, a HfSiON layer is included between said high dielectric constant insulating film and said gate electrode. Alternatively, said high dielectric constant insulating film has a multi-layered structure including one of a silicon oxide film and a silicon nitride film, and a HfSiON layer.

[0017]

More preferably, said metal M is a metal that can be silicided and applied to a low-temperature salicide process.

[0018]

More preferably, said metal M is Ni.

[0019]

More preferably, assuming that said metal M is nickel and a region of a silicide making contact with said gate insulating film is expressed as Ni_xSi_{1-X} ($0<X<1$), said X is equal to or greater than 0.6 and smaller than 1 ($0.6 \leq X<1$) in said nickel silicide contained in a gate electrode formed above a p-channel, and said X is greater than 0 and equal to or smaller than 0.5 ($0<X \leq 0.5$) in said nickel silicide contained in a gate electrode formed above a n-channel. Alternatively, said nickel silicide contained in said gate electrode formed above said p-channel contains Ni_3Si phase as a principal constituent at least in a region through which said nickel silicide makes contact with said gate insulating film, and said nickel silicide contained in said gate electrode formed above said n-channel contains one of NiSi phase and $NiSi_2$ phase as a principal constituent at least in a region through which said nickel silicide makes contact with said gate insulating film.

[0020]

In another aspect of the present invention, there is provided a semiconductor device including a silicon substrate, a gate insulating film formed on said silicon substrate, and a gate electrode formed on said gate insulating film in this order. At least a region of said gate electrode making contact with said gate insulating film is composed of silicide containing Ni_3Si phase as a principal constituent.

[0021]

In the semiconductor device, preferably, said gate insulating film includes a high dielectric constant insulating film containing one of metal oxide, metal silicate and metal oxide or metal silicate containing nitrogen therein.

[0022]

More preferably, said high dielectric constant insulating film contains one of Hf and Zr. Alternatively, a layer containing one of Hf and Zr is included between said high

dielectric constant insulating film and said gate electrode. Alternatively, said high dielectric constant insulating film has a multi-layered structure including one of a silicon oxide film and a silicon nitride film, and one of a Hf-containing layer and a Zr-containing layer. Alternatively, said high dielectric constant insulating film contains HfSiON. Alternatively, a HfSiON layer is included between said high dielectric constant insulating film and said gate electrode. Alternatively, said high dielectric constant insulating film has a multi-layered structure including one of a silicon oxide film and a silicon nitride film, and a HfSiON layer.

[0023]

More preferably, said gate electrode is included in a p-type MOSFET.

[0024]

In another aspect of the present invention, there is provided a method of fabricating a semiconductor device including: depositing poly-silicon (poly-Si) on a gate insulating film and patterning said poly-silicon into a gate electrode having desired dimension; depositing a metal M on said gate electrode; thermally annealing said gate electrode and said metal M to entirely turn said gate electrode into silicide of said metal M; and removing a portion of said metal M which was not turned into said silicide. Said metal M has such a thickness t1 above a p-channel device that, when poly-silicon and said metal M react with each other to make silicide, a portion of said silicide making contact with said gate insulating film has composition expressed with M_XSi_{1-X} ($0.5<X<1$), and has such a thickness t2 above a n-channel device that, when poly-silicon and said metal M react with each other to make silicide, a portion of said silicide making contact with said gate insulating film has composition expressed with M_XSi_{1-X} ($0<X\leq0.5$).

[0025]

Alternatively, the method includes: depositing poly-silicon on a gate insulating

film and patterning said poly-silicon into a gate electrode having desired dimension; forming a nickel (Ni) film on said gate electrode; thermally annealing said gate electrode and said nickel film to entirely turn said gate electrode to nickel silicide (NiSi); and removing a portion of said nickel film which was not turned into said nickel silicide, by etching. Said nickel film has such a thickness t1 above a p-channel device that, when poly-silicon and nickel react with each other to make nickel silicide, a portion of said nickel silicide making contact with said gate insulating film has a composition expressed as Ni_XSi_{1-X} ($0.6 \leq X < 1$), and has a thickness t2 above a n-channel device such that, when poly-silicon and nickel react with each other to make nickel silicide, a portion of said nickel silicide making contact with said gate insulating film has a composition expressed as Ni_XSi_{1-X} ($0 < X \leq 0.5$).

[0026]

Alternatively, said nickel film has such a thickness t1 above a p-channel device that, when poly-silicon and nickel react with each other to make nickel silicide, said nickel silicide has a Ni_3Si phase as a principal constituent, and has a thickness t2 above an n-channel device such that, when poly-silicon and nickel react with each other to make nickel silicide, said nickel silicide has one of a NiSi phase and a $NiSi_2$ phase as a principal constituent.

[0027]

Preferably, a ratio of a thickness T_{Ni} of said nickel film to a thickness T_{Si} of said poly-silicon is defined as $T_{Ni}/T_{Si} \geq 1.60$ to form said gate electrode including Ni_3Si phase as a principal constituent. Alternatively, a ratio of a thickness T_{Ni} of said nickel film to a thickness T_{Si} of said poly-silicon is defined as $0.55 \leq T_{Ni}/T_{Si} \leq 0.95$ to form said gate electrode including NiSi phase as a principal constituent. Alternatively, a ratio of a thickness T_{Ni} of said nickel film to a thickness T_{Si} of said poly-silicon is defined as

$0.28 \leq T_{Ni}/T_{Si} \leqq 0.54$, and said gate electrode and said nickel film are thermally annealed at 650 degrees centigrade or higher to form said gate electrode including $NiSi_2$ phase as a principal constituent.

[0028]

More preferably, the step of depositing said metal M or said nickel film includes: after forming said metal M or said nickel film above a n-channel device or a p-channel device by the thickness of t2, forming diffusion-preventing layer which is stable to said metal M or said nickel film, only above said n-channel device; and depositing said metal M or said nickel film by the thickness of (t1−t2).

[0029]

More preferably, said diffusion-preventing layer can be selectively etched relative to silicide of said metal M.

[0030]

More preferably, said diffusion-preventing layer contains one of TiN and TaN as a primary constituent.

[0031]

More preferably, said gate electrode and said metal M or said nickel film are thermally annealed for silicidation at such a temperature that a resistance of metal silicide formed in a diffusion contact region of said semiconductor device is not increased.

[0032]

In another aspect of the present invention, there is provided a method of fabricating a semiconductor device including: depositing poly-silicon on a gate insulating film and patterning said poly-silicon into a gate electrode having a desired dimension; forming a nickel (Ni) film on said gate electrode; thermally annealing said gate electrode and said nickel film to entirely turn said gate electrode into nickel silicide (NiSi); and

removing a portion of said nickel film which was not turned into said nickel silicide, by etching. A ratio of a thickness T_{Ni} of said nickel film to a thickness T_{Si} of said poly-silicon is defined as $1.60 \leq T_{Ni}/T_{Si}$.

[0033]

In the specification, the term "high dielectric constant" (High-k) is used for distinguishing from an insulating film composed of silicon dioxide (SiO2) and conventionally used as a gate insulating film, and means a higher dielectric constant than the same of an insulating film composed of silicon dioxide (SiO2). A specific numerical range of "high dielectric constant" is not to be limited.

Effects of the Invention

[0034]

In accordance with the present invention, a gate electrode is composed of silicide. This ensures avoiding depletion in a gate electrode, and makes it possible to control a work function of a gate electrode to be formed on a high dielectric constant gate insulating film by controlling composition of the silicide, though the control of a work function was said quite difficult. Accordingly, it is possible to control a threshold voltage (Vth) suitably to each of devices by applying a silicide electrode having appropriate composition to p-type and n-type MOSFETs. Since the composition of silicide is determined in a self-aligning manner in accordance with a primary crystal phase of the silicide, it would be possible to have a broad process margin, making it possible to suppress fluctuation in a threshold voltage (Vth). In addition, it is possible to avoid a contact silicide layer formed in a source/drain diffusion region from being highly resistive, by selecting a metal such as nickel applicable to a low-temperature salicide process. Since the method of fabricating a semiconductor device in accordance

with the present invention does not include a step of, after a poly-Si electrode was formed on a gate insulating film, removing the poly-Si electrode, the gate insulating film is not exposed at a surface thereof to wet-etchant or organic solvents a couple of times. Accordingly, it is possible to present a CMOSFET including a metal gate electrode and a gate insulating film having a high dielectric constant both of which are superior in reliability.

BEST MODE FOR CARRYING OUT THE INVENTION

[0035]

Hereinafter, the present invention is explained in detail based on exemplary embodiments.

[0036]

The present invention is based on the discovery that a slight change in silicide composition causes significant change in a work function when a CMOSFET is designed to include a high dielectric constant gate insulating film for enhancing the performance thereof, an n-type MOSFET is designed to have a gate electrode composed of silicon-rich silicide, and a p-type MOSFET is designed to have a gate electrode composed of metal-rich silicide.

[0037]

The above-mentioned phenomenon is relevant to pinning (which is mentioned later in the reference example 1) of an electrode Fermi-level, caused when a poly-Si electrode is formed on a HfSiON film. Such significant change in a work function cannot be obtained, if a gate insulating film is composed of SiO_2. Specifically, if a silicon-rich silicide electrode is formed, for instance, on a HfSiON film as a high dielectric constant insulating film, the influence caused by Fermi-level pinning at a

poly-Si/HfSiON interface before being silicided remains as it is without being cancelled. Thus, a work function of the silicide electrode is close to 4.1 to 4.3 eV during which Fermi-level pinning of a poly-Si electrode formed on an HfSiON film exists. In contrast, Fermi-level pinning is weaker in a silicide electrode containing a metal at a higher concentration. Thus, a work function (4.8 eV) substantially inherent to silicide is reflected onto a gate electrode.

[0038]

Furthermore, in the present invention, a metal which can completely turn poly-Si into silicide at a low temperature is used. Specifically, it is preferable to turn poly-Si into silicide at a temperature in the range of 350 to 500 degrees centigrade, because a resistance of metal silicide formed in a contact region of a source/drain diffusion layer is not increased at such a temperature. Further, a metal which is capable of forming both a silicon-rich crystal phase and a metal-rich crystal phase at 350 to 500 degrees centigrade is used. It is possible to determine a composition of a gate electrode in self-aligning manner by using the above-mentioned metal for turning a poly-Si electrode into silicide therewith, ensuring that fluctuation in a CMOS process can be suppressed. As is obvious in light of the explanation made above, nickel (Ni) is preferable as a metal M in silicide. The use of Ni makes it possible to completely turn poly-Si into silicide even when an annealing temperature is equal to or smaller than 450 degrees centigrade. Furthermore, it is further possible to gradually change a composition of crystal phase by changing Ni supply. It is preferable for the above-mentioned reasons that, assuming that a region of nickel silicide making contact with a HfSiON film is expressed as Ni_xSi_{1-X} ($0<X<1$), X is equal to or greater than 0.6, but smaller than 1 ($0.6 \leq X<1$) in Ni silicide of which a gate electrode is composed in a p-type MOSFET, and X is greater than 0 and equal to or smaller than 0.5 ($0<X \leq 0.5$) in Ni

silicide of which a gate electrode is composed in a n-type MOSFET. It is more preferable that, assuming that a region of nickel silicide making contact with a HfSiON film is expressed as Ni_xSi_{1-X} ($0<X<1$), X is greater than 0.6, but smaller than 0.8 ($0.6<X<0.8$) in Ni silicide of which a gate electrode is composed in a p-type MOSFET, and X is greater than 0.3 and smaller than 0.55 ($0.3<X<0.55$) in Ni silicide of which a gate electrode is composed in a n-type MOSFET. This is because crystal phases of Ni are grouped primarily into $NiSi_2$, NiSi, Ni_3Si_2, Ni_2Si and Ni_3Si, and these compounds can be formed with use of thermal history. It is most preferable that, assuming that a region of nickel silicide making contact as a HfSiON film is expressed as Ni_xSi_{1-X} ($0<X<1$), X is greater than 0.7, but smaller than 0.8 ($0.7<X<0.8$) in Ni silicide of which a gate electrode is composed in a p-type MOSFET, and X is greater than 0.45 and smaller than 0.55 ($0.45<X<0.55$) in Ni silicide of which a gate electrode is composed in an n-type MOSFET. That is, it is preferable that silicide contained in a gate electrode in a p-type MOSFET primarily contains Ni_3Si phase, and silicide contained in a gate electrode in an n-type MOSFET primarily contains a NiSi phase. FIG. 1 illustrates the structure of a CMOS transistor

[0039]

The metal M is not limited to Ni. As the metal M, there may be used tantalum (Ta), platinum (Pt), cobalt (Co), titanium (Ti), hafnium (Hf), vanadium (V), chromium (Cr), zirconium (Zr) or niobium (Nb), for instance, if they can turn poly-Si into silicide at a temperature at which a resistance of metal silicide formed in a contact area in a source/drain diffusion layer is not increased, and further if it is possible to form both silicon-rich crystal phase and metal-rich crystal phase at the temperature.

[0040]

Furthermore, in the present invention, a gate electrode contains silicide of metal M as a primary constituent, expressed as M_xSi_{1-X} ($0<X<1$), and X is greater than 0.5 ($X>0.5$) in the silicide of metal M contained in a gate electrode formed above a p-channel, and X is equal to or smaller than 0.5 ($X\leq0.5$) in the silicide of metal M contained in a gate electrode formed above a n-channel.

[0041]

The use of the metal silicide meeting the above-mentioned conditions makes it possible not only to suppress a reduction in a drain current in a transistor, caused by depletion of a conventionally used gate electrode composed of poly-Si, but also to provide the following advantages. (1) It is possible to control a work function in a high dielectric constant gate insulating film, though the work function control was quite difficult in a conventional silicide electrode. (2) Since it is possible to control silicide composition with crystal phases of silicide, and further it is possible to control crystal phases of silicide with a thickness of a metal film formed on poly-Si, large margin in fabrication conditions is ensured, and reproducibility of transistors can be enhanced. (3) The use of metal-rich silicide can make a range in which a work function is modulated broader than mid-gap of silicon. (4) The use of metal-rich silicide can make it possible to select a low-temperature silicidation process. (5) Since it is not necessary to change constituent composition of a gate electrode, it is no longer necessary to carry out a step of etching for removal a film deposited on a gate insulating film unlike in a conventional process. This ensures it is possible to prevent a gate insulating film from being damaged by etching. (6) It is possible to carry out a salicide process in a silicide fabrication process, ensuring simplification in steps of fabricating a gate electrode.

[0042]

In the explanation made above, a composition of a gate electrode and a profile

of crystal phase in a depth-wise direction are not mentioned. However, since a threshold voltage (Vth) of a MOSFET is dependent on a combination of a gate insulating film and a gate electrode disposed adjacent thereto, if constituents, composition and/or crystal phases in a region at which a gate electrode and a gate insulating film make contact with each other meet the conditions required in the present invention, it would be possible to obtain the advantages of the present invention, even if constituents and/or crystal phases in a region of a gate electrode not making contact with a gate insulating film are different from the above-mentioned ones, and even if a gate electrode has a composition varying in a depth-wise direction.

[0043]

Embodiments in accordance with the present invention are explained hereinafter with reference to the drawings.

[Embodiments]

[0044]

Embodiment 1

FIGS. 3 (a) to (g) and FIGS. 4A to 4J are cross-sectional views each showing a step of a method of fabricating a CMOSFET in accordance with the embodiment 1. In the present embodiment, MOSFETs are fabricated by means of CMP (Chemical Mechanical Polishing) for polishing an interlayer insulating film to be planarized, after having been formed, and simultaneously exposing upper portions of the gate electrodes.

[0045]

First, as illustrated in FIG. 3 (a), element isolation regions 2 are formed on a surface of the silicon substrate 1 by means of STI (Shallow Trench Isolation) process. Then, a gate insulating film 3 is formed on a surface of the silicon substrate 1 isolated by the element isolation region 2. The gate insulating film 3 is comprised of a high

dielectric constant insulating film composed of metal oxide, metal silicate, metal oxide into which nitrogen is doped, or metal silicate into which nitrogen is doped. In particular, it is preferable that the gate insulating film 3 contain Hf or Zr. This is because an electrically insulating film containing Hf or Zr is stable for annealing to be carried out at a high temperature, and it is possible for the film to contain a small amount of fixed electric charges therein. Furthermore, it is preferable to form a layer containing Hf or Zr such that the layer makes contact with a gate electrode comprised of a high dielectric constant insulating film. This is because a threshold voltage of a MOSFET is dependent on a combination of a gate electrode and a high dielectric film making contact with the gate electrode. A silicon oxide film or a silicon oxide nitride film may be formed between the electrically insulating film and the silicon substrate 1 in order to reduce an interfacial level at an interface between the silicon substrate 1 and the gate insulating film 3 and further reduce the influence caused by fixed electric charges included in the electrically insulating film. A HfSiON film, the silicon oxide film or a HfSiON film on the silicon oxide nitride film are more preferable. In the embodiment 1, a concentration of Hf in the gate insulating film 3 varies in a depth-wise direction thereof. The HfSiON layer 18 has a highest concentration of Hf in the vicinity of an interface between the gate electrode and the gate insulating film 3, and has a composition of a thermally oxidized silicon film in the vicinity of an interface between the silicon substrate 1 and the gate insulating film 3. In order to obtain the HfSiON film 18 having the above-mentioned structure, a thermally oxidized silicon film having the thickness of 1.9 nm is first formed. Then, Hf having the thickness of 0.5 nm is deposited on the thermally oxidized silicon film by a long-throw sputtering process. Then, the resultant is thermally annealed twice, first at 500 degrees centigrade in oxygen atmosphere for one minute, and second at 800 degrees centigrade in nitrogen atmosphere for thirty seconds.

This results in Hf being diffused into the underlying silicon oxide film in solid phase, and thereby a HfSiON film is formed. Thereafter, the HfSiON film is annealed at 900 degrees centigrade in a NH_3 atmosphere for ten minutes to thereby fabricate the HfSiON film.

[0046]

Then, a multi-layered structure comprised of the poly-silicon (poly-Si) film 4 having a thickness of 40 nm and the silicon oxide film 5 having a thickness of 150 nm is formed on the gate insulating film. As illustrated in FIG. 3 (b), the multi-layered structure is patterned into a gate electrode by lithography and reactive ion etching (RIE). Then, ions are doped into the silicon substrate 1 with the gate electrode being used as a mask to thereby form the extended diffusion layer region 6 around the gate electrode in a self-aligning manner.

[0047]

Then, as illustrated in FIG. 3 (c), a silicon oxide film and a silicon nitride film are successively formed. Then, those films are etched back to thereby form the gate sidewall 7. Then, ions are doped again into the silicon substrate 1. Then, the silicon substrate 1 is annealed for activating the ions to form the source/drain diffusion layers 8.

[0048]

Then, as illustrated in FIG. 3 (d), a metal film 9 having the thickness of 20 nm is formed entirely on the silicon substrate by sputtering. Then, a silicide layer 10 having the thickness of about 40 nm is formed in accordance with the salicide process only at areas disposed above the source/drain diffusion layers with the gate electrode, the gate sidewall and the STI being used as a mask (FIG. 3 (e)). The silicide layer 10 is composed of Ni mono-silicide (NiSi) for minimizing a contact resistant thereof. In place of Ni silicide, the silicide layer 10 may be composed of Co silicide or Ti silicide.

[0049]

Then, as illustrated in FIG. 3 (f), an interlayer insulating film 11 comprised of a silicon oxide film is formed entirely on the silicon substrate by CVD (Chemical Vapor Deposition). Then, as illustrated in FIG. 3 (g), the interlayer insulating film 11 is flattened by CMP. Then, the interlayer insulating film 11 is etched back to make the poly-silicon film 4 of the gate electrode exposed.

[0050]

Then, as illustrated in FIG. 4 (h), a first metal film 12 is formed entirely on the silicon substrate 1 for making silicide of the gate electrode and the poly-silicon film 4. A metal of which the first metal film 12 is composed is selected from metals which make silicide with the poly-silicon film 4, for instance, selected from Ni, Pt, Hf, V, Ti, Ta, W, Co, Cr, Zr, Mo, Nb or alloys thereof. It is preferable to select a metal which is capable of turning the poly-silicon film 4 into silicide at such a temperature that a resistance of the silicide layer 10 formed in the source/drain diffusion layers 8 is not increased. For instance, if a nickel mono-silicide (NiSi) layer is formed in the source/drain diffusion layers 8, it would be necessary to carry out the subsequent process at 500 degrees centigrade or lower in order to prevent a contact resistance between the source/drain diffusion layers 8 and wirings from increasing due to disilicidation of nickel (NiSi2). Accordingly, nickel is selected in the embodiment 1, because silicidation can be well accomplished at 500 degrees centigrade of lower. The first metal film 12 composed of nickel is formed so as to have such a thickness t2 that when the poly-silicon film 4 and nickel sufficiently react with each other into silicide, a portion of the silicide making contact with the gate insulating film 3 has a composition defined as Ni_xSi_{1-X} ($0<X\leq0.5$). It is preferable that the first metal film 12 have such a thickness that the silicide film to be formed after the silicidation contains a NiSi phase or a $NiSi_2$ phase as a primary

constituent. This is because a work function of the silicide film containing NiSi phase or $NiSi_2$ phase as a primary constituent can be set in the range of 4.4 to 4.5 eV relative to HfSiON. In the embodiment 1, a nickel film having the thickness of 22 nm is formed at room temperature by DC magnetron sputtering.

[0051]

A diffusion-preventing layer 13 is formed entirely on the first metal film 12 comprised of a nickel film. A material of which the diffusion-preventing layer 13 is composed is selected from materials which can prevent the diffusion of metal to be turned into silicide in a thermally annealing step to be carried out for completely turning gate poly-silicon into silicide, and which is also stable. It is preferable that the diffusion-preventing layer 13 can selectively be etched in selected areas relative to the silicided metal and the interlayer insulating film 11, because the process of fabricating a transistor can be simplified. In the embodiment 1, a TiN film having the thickness of 20 nm is formed at 300 degrees centigrade by reactive sputtering.

[0052]

Then, as illustrated in FIG. 4 (i), only the TiN film disposed above the Ni film in the p-type MOSFET is removed by lithography and RIE. Then, a second metal film 14 identical in constituent with the first metal film 12 is formed entirely on the silicon substrate for making silicide. In the embodiment 1,nickel is formed. The nickel film is designed to have such a thickness t1 that when the poly-silicon film 4 sufficiently reacts with nickel to thereby turn into silicide, a portion of the silicide making contact with the gate insulating film has a composition defined as Ni_xSi_{1-X} ($0.5<X<1$). It is preferable that the second metal film 14 have such a thickness t1 that a portion of the silicide making contact with the gate insulating film 3 has a composition defined as Ni_xSi_{1-X} ($0.6\leq X<1$). This is because nickel silicide including nickel whose composition

amount is twice or more greater than that of silicon has a work function of 4.6 eV on HfSiON. It is more preferable that the second metal film 14 have such a thickness t1 that the resultant silicide includes a Ni_3Si phase as a primary constituent. This is because silicide including a Ni_3Si phase as a primary constituent has a work function of 4.8 eV on HfSiON. In the embodiment 1, a nickel film having the thickness of 44 nm is formed at room temperature by DC magnetron sputtering. Accordingly, a nickel film having a total thickness of 66 nm contributes to the silicidation above the gate insulating film 3 in the p-type MOSFET, whereas only a nickel film having a thickness of 22 nm disposed beneath the diffusion-preventing layer 13 contributes to the silicidation above the gate insulating film 3 in the n-type MOSFET.

[0053]

Then, a thermally annealing step is carried out for turning the poly-silicon film 4 formed on the gate insulating film 3, the first metal film 12, and the second metal film 14 into silicide. It is necessary to carry out the thermally annealing step in a non-oxidizing atmosphere in order to prevent the metal films from being oxidized. At the same time, it is further necessary to carry out the thermal annealing step at a temperature such that a sufficient diffusion speed can be accomplished for entirely turning the poly-silicon film 4 formed on the gate insulating film 3 into silicide, and the silicide layer 10 formed in the source/drain diffusion layers 8 does not become highly resistive. In the embodiment 1, since the silicide layer 10 formed on the source/drain diffusion layers 8 and the silicide formed on the gate electrode are both nickel silicide, the above-mentioned thermal annealing is carried out at 450 degrees centigrade in a nitrogen gas atmosphere for two minutes. The above-mentioned thermal annealing may be carried out at a higher temperature, if the silicide layer 10 formed on the source/drain diffusion layers 8 is Co silicide or Ti silicide. For instance, the thermal annealing may be carried out at 800

degrees centigrade. As a result of carrying out the above-mentioned thermal annealing, the poly-silicon film having the thickness of 40 nm reacts with the nickel film having a thickness of 22 nm to thereby turn into silicide above the gate insulating film 3 in the n-type MOSFET. On the other hand, the poly-silicon film having the thickness of 40 nm reacts with the nickel films having the thickness of 66 nm to thereby turn into silicide above the gate insulating film 3 in the p-type MOSFET. Since a larger amount of nickel can be supplied to the poly-silicon film 4 in the p-type MOSFET than in an n-type MOSFET, the Ni silicide gate electrode 16 contains nickel in a higher concentration than the Ni silicide gate electrode 15 of the n-type MOSFET. As shown in FIG. 12 illustrating wave-forms indicating the measurement results of X-ray diffraction (XRD) and Rutherford back-scattering (RBS), the nickel silicide gate electrode 15 of the n-type MOSFET is comprised only of NiSi phase, and a composition ratio Ni/(Ni+Si) is about 0.5. In contrast, the nickel silicide gate electrode 16 of the p-type MOSFET is comprised of combined phases of NiSi and Ni_3Si as a main phase, and a composition ratio Ni/(Ni+Si) is about 0.75.

[0054]

Then, portions of the nickel film and the TiN film which do not contribute to silicidation in the thermally annealing step are removed by wet etching through the use of aqueous solution of sulfuric acid hydrogen peroxide.

[0055]

In the above-mentioned steps, peeling of the gate electrodes was not observed at all.

[0056]

By carrying out the above-mentioned steps, there is fabricated a CMOSFET including the nickel full-silicide electrodes having different compositions from each

other in the n-type and p-type MOSFETs, as illustrated in FIG. 4 (j). As shown in Table 1, a crystal phase of nickel silicide is dependent on a thickness of the nickel film formed on the poly-silicon film, that is, an amount of nickel to be supplied to the poly-silicon film.

[0057]

[Chart 1]

CHART 1

		T_{Ni}/T_{Si}			
		0.33	0.67	1.20	1.80
ANEAL TEMPERATURE (°C)	650	$NiSi_2$+NiSi			
	600	NiSi			
	500	NiSi	NiSi		$NiSi+Ni_3Si$
	450		NiSi		$NiSi+Ni_3Si$
	400		NiSi	NiSi	$NiSi+Ni_3Si$

The inventors discovered that when a gate electrode of an n-type MOSFET is comprised of NiSi phase, a ratio (T_{Ni}/T_{Si}) between a thickness (T_{Si}) of a gate poly-silicon film and a thickness (T_{Ni}) of a nickel film is preferably in the range of 0.55 to 0.95, and when a gate electrode of a p-type MOSFET is comprised of silicide containing $NiSi_3$ phase as a primary constituent, the ratio (T_{Ni}/T_{Si}) is preferably equal to or greater than 1.60. However, when a gate electrode is comprised of silicide containing $NiSi_2$ phase as a primary constituent, it is necessary to determine the ratio (T_{Ni}/T_{Si}) in the range of 0.28 to 0.54, and to turn poly-silicon into silicide at 650 degrees centigrade or greater. Furthermore, since the composition Ni/(Ni+Si) on which a work function of nickel

silicide is dependent is determined by crystal phases such as $NiSi_2$, NiSi, Ni_2Si or Ni_3Si almost in self-aligning manner, it is possible to ensure wide margin in process conditions such as the total thickness of deposited nickel films or a temperature at which poly-silicon is turned into silicide both for providing common crystal phase (that is, an identical work function), and to reduce fluctuation in fabrication process. In accordance with the above-mentioned steps, it is possible to fabricate a CMOSFET including n-type and p-type MOSFETS having gate electrodes composed of Ni silicide wherein composition ratios of the gate electrodes are different from each other, and a nickel concentration of the nickel silicide gate electrode of the p-type MOSFET is higher than that of the nickel silicide gate electrode of the n-type MOSFET.

[0058]

FIG. 5 is a graph showing a relationship between a gate capacity (C) and a gate voltage (V) in a CMOSFET including the gate insulating film comprised of a HfSiON film that is a high dielectric constant material.

[0059]

FIG. 6 is a graph showing a relationship between a work function estimated based on a flat band voltage and a composition ratio of a Ni silicide gate electrode. The compositions Ni/(Ni+Si) associated with the three solid circles illustrated in FIG. 6 indicate $NiSi_2$, NiSi and Ni_3Si, respectively, from the left to the right. It is understood that a work function of nickel silicide formed on a HfSiON film is determined in association with a composition ratio of a nickel silicide gate electrode determined by these crystal phases in a self-aligning manner. Specifically, work functions of NiSi and Ni_3Si are 4.5 eV and about 4.8 eV, respectively.

[0060]

FIG. 7 is a graph showing a relation between a threshold voltage (Vth) of a

CMOSFET and an amount of channel impurities. That is, it is understood that a nickel silicide gate electrode composed of NiSi is applicable to an n-type MOSFET, and a nickel silicide gate electrode composed of Ni_3Si is applicable to a p-type MOSFET.

[0061]

FIG. 8 is a graph showing the dependency of a drain current on a gate voltage in an n-type MOSFET having a Ni silicide gate electrode. FIG. 9 is a graph showing electron mobility of an n-type MOSFET. As can be understood from the drawings, a threshold voltage (Vth) of an n-type MOSFET including a nickel silicide gate electrode is equal to a threshold voltage (Vth) having been estimated with reference to FIG. 7. In addition, the carrier mobility of the transistor is equal to carrier mobility of a poly-Si/SiO2 transistor.

[0062]

As is obvious in light of the explanation made above, a combination of the NiSi gate electrode and the HfSiON gate insulating film, shown in the embodiment 1, could present superior transistor performances.

[0063]

Reference Example 1

As a reference example 1 of the embodiment 1, a structure including the gate insulating film composed of a high dielectric constant material and the gate electrode composed of poly-silicon is formed as illustrated in FIG. 2 (a). The same steps as those carried out until the gate insulating film was formed in the embodiment 1 were carried out to form the structure. Then, poly-silicon was deposited over the silicon substrate, and subsequently, the poly-silicon was etched into the gate electrodes without forming the interlayer insulating film on the poly-silicon. Then, the gate sidewall was formed in the same way as the embodiment 1. When the source/drain diffusion layers were

formed, impurities were doped into the poly-silicon of which the gate electrodes were composed. Specifically, phosphorus (P) was doped into the poly-silicon electrode of the n-type MOSFET at 3E15 (cm^{-2}), and boron (B) was doped into the poly-silicon electrode of the p-type MOSFET at 3E15 (cm^{-2}). After activation of the impurities, nickel silicide was formed on the source/drain diffusion layers and the poly-silicon gate electrodes by means of a salicide process, similarly to the embodiment 1. The nickel silicide formed on the gate electrodes does not reach the gate insulating film.

[0064]

FIG. 10 is a graph showing a relation between a gate capacity (C) and a gate voltage (V) in the fabricated p-type MOSFET. Since the gate electrodes were composed of poly-silicon, depletion occurred in the electrodes, and capacity reduction further occurred in an inverted region which was equivalent to about a 5 angstrom increase of EOT. Furthermore, pinning of electrode Fermi-level occurred at an interface between the electrodes and an insulating film due to defects at an interface between the poly-silicon and the high dielectric constant gate insulating film, resulting in a problem that a threshold voltage of a transistor could not be controlled. A work function of poly-silicon obtained by a flat band voltage illustrated in FIG. 8 in the case that a gate insulating film was composed of HfSiON was not dependent on doped impurity, but was fixed around 4.1 to 4.3 eV, resulting in that a threshold voltage (Vth) of the p-type MOSFET was relatively high, specifically in the range of about -1.0 to about -0.8 V.

[0065]

Reference Example 2

As a reference example of the embodiment 1, the gate insulating film was comprised of a film composed of thermally oxidized silicon, and the gate electrodes were comprised of NiSi electrodes as a metal gate electrode in order to avoid depletion of a

gate electrode, as illustrated in FIG. 2 (b). The gate insulating film was comprised of a thermally oxidized film having a thickness of 3 nm. After the processes up to the step illustrated in FIG. 1 (g) were carried out in the same way as the embodiment 1, impurity was doped into gate poly-silicon, and then, was annealed for activation. The annealing was carried out in the same conditions as those of the embodiment 2 except the impurity-doping conditions. A dosed amount of phosphorus (P) and boron (B) was in the range of 0 to 5E20 (cm^{-3}). After nickel which obtained the ratio of T_{Ni}/T_{Si} equal to 0.55 had been deposited in the same way as the embodiment 1, the gate poly-silicon was annealed at 450 degrees centigrade for two minutes to thereby make nickel silicide. The gate electrodes were comprised fully of NiSi phase. Then, an excessive portion of the nickel was etched for removal.

[0066]

FIG. 11 is a graph showing the dependency of a work function of a NiSi electrode formed on a SiO_2 film on doses of impurities, the dependency being determined based on the C-V curves. It has been understood that a work function could be varied within a range of 4.4 to 4.7 eV by changing an impurity to another and/or varying a dose of impurity. Accordingly, it is possible to avoid depletion of a gate electrode through the use of a NiSi electrode into which an impurity is doped, and thus, it is possible to fabricate a metal gate CMOSFET superior in threshold voltage (Vth) control almost without changing the structure of a conventional CMOSFET. The above-mentioned advantages can be obtained when a gate insulating film is composed of silicon dioxide. The advantages cannot be obtained in a CMOSFET working with low power consumption, in which it is necessary to reduce a gate leakage current.

[0067]

In order to solve the problem, a CMOSFET was fabricated in which the gate

insulating film was replaced with an element having the multi-layered structure, mentioned in the embodiment 1, comprised of a thermally oxidized silicon film and a HfSiON film formed on the thermally oxidized silicon film. FIG. 11 is a graph showing the dependency of a work function of a NiSi electrode formed on a HfSiON film, on doses of impurities, the dependency being determined based on the C-V curves. A work function of the NiSi electrode formed on the HfSiON film is constantly equal to 4.5 eV regardless of a dose. Thus, it has been understood that it was not possible to control a work function of the NiSi electrode formed on the HfSiON film by varying a dose of impurity contained in NiSi. Accordingly, a threshold voltage in a p-type MOSFET which is high due to Fermi pining occurring at an interface between a poly-silicon film and a HfSiON film can be lowered only by about 0.1 V, and hence, it is not possible to accomplish a threshold voltage required in CMOSFET working with low power consumption.

[0068]

While the present invention has been described in connection with certain embodiments, it is to be understood that the present invention is not limited to those specific embodiments. On the contrary, various modifications of the present invention can be made without departing from the spirit and scope of the following claims.

[0069]

For instance, as mentioned in the embodiment 1, the combination of a metal with which a gate electrode is turned into silicide and a metal with which source/drain diffusion layers are turned into silicide is required to meet the condition that gate poly-silicon can be turned into silicide at such a temperature that the silicide of which the source/drain diffusion layers are composed is not altered. By managing the conditions such as an annealing temperature or time for carrying out annealing in accordance with a

combination of metals used for silicidation, it would be possible to have desired advantages. For instance, even if it is quite difficult to accomplish silicidation at a low temperature with a certain metal, it would be sometimes possible to accomplish silicidation with the certain metal by carrying out annealing for a long time. Furthermore, it is also possible to lower a temperature at which silicidation can be accomplished, by replacing poly-silicon formed on a gate insulating film with amorphous silicon, or controlling a temperature at which a metal film to be turned into silicide is formed. If necessary, the replacement of poly-silicon with amorphous silicon and the temperature control are both carried out.

BRIEF DESCRIPTION OF THE DRAWINGS

[0070]

FIG. 1 is a cross-sectional view of a semiconductor device of the present invention.

FIG. 2 (a) to 2 (c) are cross-sectional views of a conventional semiconductor device in accordance with an embodiment of the present invention.

FIGS. 3 (a) to 3 (g) are cross-sectional views illustrating a process of the method of fabricating the semiconductor device in accordance with the embodiment of the present invention.

FIGS. 4 (a) to 4 (g) are cross-sectional views illustrating a process of the method of fabricating the semiconductor device in accordance with the embodiment of the present invention.

FIG. 5 illustrates wave-forms indicating the measurement results of a C-V curve of the semiconductor device fabricated in accordance with the first embodiment.

FIG. 6 is a graph showing a work function of a composition of a Ni silicide gate

electrode.

FIG. 7 is a graph showing a range of a threshold voltage of a transistor accomplished by a work function of a Ni silicide gate electrode fabricated in accordance with the embodiment.

FIG. 8 is a graph showing the dependency of a drain current on a gate voltage in an n-type MOSFET fabricated in accordance with the embodiment.

FIG. 9 is a graph showing the measurement results of electron mobility of the n-type MOSFET fabricated in accordance with the first embodiment.

FIG. 10 is a graph showing the measurement results of a C-V curve of the conventional p-type MOSFET including a poly-silicon gate electrode and a HfSiON gate insulating film.

FIG. 11 is a graph showing the effect of implanting impurities into gate electrodes with respect to a work function obtained from the C-V curves of the conventional p-type and n-type MOSFETs including Ni silicide as the gate electrode, and SiO_2 and HSiON as the gate insulating film.

FIG. 12 illustrates wave-forms indicating the measurement results of X-ray diffraction in each of crystal phases of Ni silicide of the present invention.

Description of Reference Numerals

[0071]

1 silicon substrate

2 element isolation region

3 and 28 gate insulating film

4 poly-silicon film

5 silicon oxide film

6 extension diffusion region

7 and 29 gate wall

8 source/drain diffusion layer

9 metal film

10 silicide layer

11 interlayer insulating film

12 first metal film

13 diffusion preventing layer

14 second metal layer

15 NiSi electrode

16 Ni_3Si electrode

17 SiO_2

18 HfSiON

19 Ni_xSi_{1-x} ($0<x\leq0.5$) gate electrode

20 Ni_xSi_{1-x} ($0.6\leq x<1$) gate electrode

21 n^+-poly-Si electrode

22 p^+-poly-Si electrode

23 P doped NiSi electrode

24 B doped NiSi electrode

25 W silicide film

26 W film

27 W film

CLAIMS

1. A semiconductor device comprising a silicon substrate, a gate insulating film formed on said silicon substrate, and a gate electrode formed on said gate insulating film, in this order, wherein:

said gate insulating film includes an electrically insulating film having a high dielectric constant and containing one of metal oxide, metal silicate and metal oxide or metal silicate containing nitrogen therein;

said gate electrode contains a silicide of metal X as a primary constituent, and has a region through which said gate electrode makes contact with said gate insulating film and which has a composition expressed as M_xSi_{1-X} ($0<X<1$); and

X is greater than 0.5 ($X>0.5$) in said metal M contained in a gate electrode formed above a p-channel, and X is equal to or smaller than 0.5 ($X\leq0.5$) in said metal M contained in a gate electrode formed above a n-channel.

2. The semiconductor device as set forth in claim 1, wherein said electrically insulating film contains one of Hf and Zr.

3. The semiconductor device as set forth in claim 1, further comprising a layer containing one of Hf and Zr therein between said electrically insulating film and said gate electrode.

4. The semiconductor device as set forth in claim 1, wherein said electrically insulating film has a multi-layered structure including one of a silicon oxide film and a silicon nitride film, and one of a Hf-containing layer and a Zr-containing layer.

5. The semiconductor device as set forth in claim 1, wherein said electrically insulating film contains HfSiON.

6. The semiconductor device as set forth in claim 1, further comprising a HfSiON layer between said electrically insulating film and said gate electrode.

7. The semiconductor device as set forth in claim 1, wherein said electrically insulating film has a multi-layered structure including one of a silicon oxide film and a silicon nitride film, and a HfSiON layer.

8. The semiconductor device as set forth in claims 1 to 7, wherein said metal M is a metal that can be silicided and applied to a low-temperature salicide process.

9. The semiconductor device as set forth in claims 1 to 7, wherein said metal M is Ni.

10. The semiconductor device as set forth in claim 9, wherein assuming that said metal M is nickel and a region of a silicide making contact with said gate insulating film is expressed as Ni_xSi_{1-X} ($0<X<1$), X is equal to or greater than 0.6 and smaller than 1 ($0.6 \leq X<1$) in said nickel silicide contained in a gate electrode formed above a p-channel, and X is greater than 0 and equal to or smaller than 0.5 ($0<X \leq 0.5$) in said nickel silicide contained in a gate electrode formed above a n-channel.

11. The semiconductor device as set forth in claim 9, wherein said nickel silicide

contained in said gate electrode formed above said p-channel contains Ni_3Si phase as a principal constituent at least in a region through which said nickel silicide makes contact with said gate insulating film, and said nickel silicide contained in said gate electrode formed above said n-channel contains one of NiSi phase and $NiSi_2$ phase as a principal constituent at least in a region through which said nickel silicide makes contact with said gate insulating film.

12. A semiconductor device comprising a silicon substrate, a gate insulating film formed on said silicon substrate, and a gate electrode formed on said gate insulating film, wherein at least a region of said gate electrode making contact with said gate insulating film is composed of silicide containing Ni_3Si phase as a principal constituent.

13. The semiconductor device as set forth in claim 12, wherein said gate insulating film includes an electrically insulating film having a high dielectric constant and containing one of metal oxide, metal silicate and metal oxide or metal silicate containing nitrogen therein.

14. The semiconductor device as set forth in claim 13, wherein said electrically insulating film contains one of Hf and Zr.

15. The semiconductor device as set forth in claim 13, further comprising a layer containing one of Hf and Zr therein between said electrically insulating film and said gate electrode.

16. The semiconductor device as set forth in claim 13, wherein said electrically

insulating film has a multi-layered structure including one of a silicon oxide film and a silicon nitride film, and one of a Hf-containing layer and a Zr-containing layer.

17. The semiconductor device as set forth in claim 13, wherein said electrically insulating film contains HfSiON.

18. The semiconductor device as set forth in claim 13, further comprising a HfSiON layer between said electrically insulating film and said gate electrode.

19. The semiconductor device as set forth in claim 13, wherein said electrically insulating film has a multi-layered structure including one of a silicon oxide film and a silicon nitride film, and a HfSiON layer.

20. The semiconductor device as set forth in claims 12 to 19, wherein said gate electrode is included in a p-type MOSFET.

21. A method of fabricating a semiconductor device, comprising:

depositing poly-silicon (poly-Si) on a gate insulating film and patterning said poly-silicon into a gate electrode having desired dimension;

depositing a metal M on said gate electrode;

thermally annealing said gate electrode and said metal M to entirely turn said gate electrode to silicide of said metal M; and

removing a portion of said metal M which was not turned into said silicide, wherein

said metal M has a thickness t1 above a p-channel device such that, when

poly-silicon and said metal M react with each other to make silicide, a portion of said silicide making contact with said gate insulating film has a composition expressed as M_XSi_{1-X} ($0.5<X<1$), and has a thickness t2 above a n-channel device such that, when poly-silicon and said metal M react with each other to make silicide, a portion of said silicide making contact with said gate insulating film has composition expressed with M_XSi_{1-X} ($0<X\leq0.5$).

22. A method of fabricating a semiconductor device, comprising:

depositing poly-silicon on a gate insulating film and patterning said poly-silicon into a gate electrode having desired dimension;

forming a nickel (Ni) film on said gate electrode;

thermally annealing said gate electrode and said nickel film to entirely turn said gate electrode into nickel silicide (NiSi); and

removing a portion of said nickel film which was not turned into said nickel silicide, by etching, wherein

said nickel film has a thickness t1 above a p-channel device such that, when poly-silicon and nickel react with each other to make nickel silicide, a portion of said nickel silicide making contact with said gate insulating film has composition expressed with Ni_XSi_{1-X} ($0.6\leq X<1$), and has a thickness t2 above a n-channel device such that, when poly-silicon and nickel react with each other to make nickel silicide, a portion of said nickel silicide making contact with said gate insulating film has a composition expressed as Ni_XSi_{1-X} ($0<X\leq0.5$).

23. A method of fabricating a semiconductor device, comprising:

depositing poly-silicon on a gate insulating film and patterning said poly-silicon

into a gate electrode having desired dimensions;

forming a nickel (Ni) film on said gate electrode;

thermally annealing said gate electrode and said nickel film to entirely turn said gate electrode into nickel silicide (NiSi); and

removing a portion of said nickel film which was not turned into said nickel silicide, by etching, wherein

said nickel film has a thickness t1 above a p-channel device such that, when poly-silicon and nickel react with each other to make nickel silicide, said nickel silicide has Ni_3Si phase as a principal constituent, and has a thickness t2 above an n-channel device such that, when poly-silicon and nickel react with each other to make nickel silicide, said nickel silicide has one of NiSi phase and $NiSi_2$ phase as a principal constituent.

24. The method as set forth in claim 23, wherein a ratio of a thickness T_{Ni} of said nickel film to a thickness T_{Si} of said poly-silicon is defined as $T_{Ni}/T_{Si} \geq 1.60$ to form said gate electrode including Ni_3Si phase as a principal constituent.

25. The method as set forth in claim 23, wherein a ratio of a thickness T_{Ni} of said nickel film to a thickness T_{Si} of said poly-silicon is defined as $0.55 \leq T_{Ni}/T_{Si} \leq 0.95$ to form said gate electrode including NiSi phase as a principal constituent.

26. The method as set forth in claim 23, wherein a ratio of a thickness T_{Ni} of said nickel film to a thickness T_{Si} of said poly-silicon is defined as $0.28 \leq T_{Ni}/T_{Si} \leqq 0.54$, and said gate electrode and said nickel film are thermally annealed at 650 degrees centigrade or higher to form said gate electrode including $NiSi_2$ phase as a principal constituent.

27. The method as set forth in claims 21 to 23, wherein the step of depositing said metal M or said nickel film comprises:

after forming said metal M or said nickel film having the thickness of t2 above a n-channel device or a p-channel device, forming diffusion-preventing layer which is stable to said metal M or said nickel film, only above said n-channel device; and

depositing said metal M or said nickel film by the thickness of (t1−t2).

28. The method as set forth in claim 27, wherein said diffusion-preventing layer can be selectively etched relative to silicide of said metal M.

29. The method as set forth in claim 27, wherein said diffusion-preventing layer contains one of TiN and TaN as a primary constituent.

30. The method as set forth in claims 21 to 29, wherein said gate electrode and said metal M or said nickel film are thermally annealed for silicidation at such a temperature that a resistance of metal silicide formed in a diffusion contact region of said semiconductor device is not increased.

31. The method as set forth in claims 12 to 20, comprising:

depositing poly-silicon on a gate insulating film and patterning said poly-silicon into a gate electrode having desired dimension;

forming a nickel (Ni) film on said gate electrode;

thermally annealing said gate electrode and said nickel film to entirely turn said gate electrode into nickel silicide (NiSi); and

removing a portion of said nickel film which was not turned into said nickel silicide, by etching, wherein

a ratio of a thickness T_{Ni} of said nickel film to a thickness T_{Si} of said poly-silicon is defined as $1.60 \leq T_{Ni}/T_{Si}$.

ABSTRACT

There is provided a semiconductor device which is capable of solving a problem of threshold control in CMOS transistor, accompanied with combination of a high dielectric constant gate insulating film and a metal gate electrode, and significantly enhancing performances without deterioration in reliability of a device. The semiconductor device includes a gate insulating film composed of a high dielectric constant material, and a gate electrode. A portion of the gate electrode making contact with the gate insulating film has a composition including silicide of metal M expressed as M_xSi_{1-X} ($0<X<1$), as a primary constituent. X is greater than 0.5 ($X>0.5$) in a p-type MOSFET, and is equal to or smaller than 0.5 ($X\leq 0.5$) in an n-type MOSFET.

FIG. 1

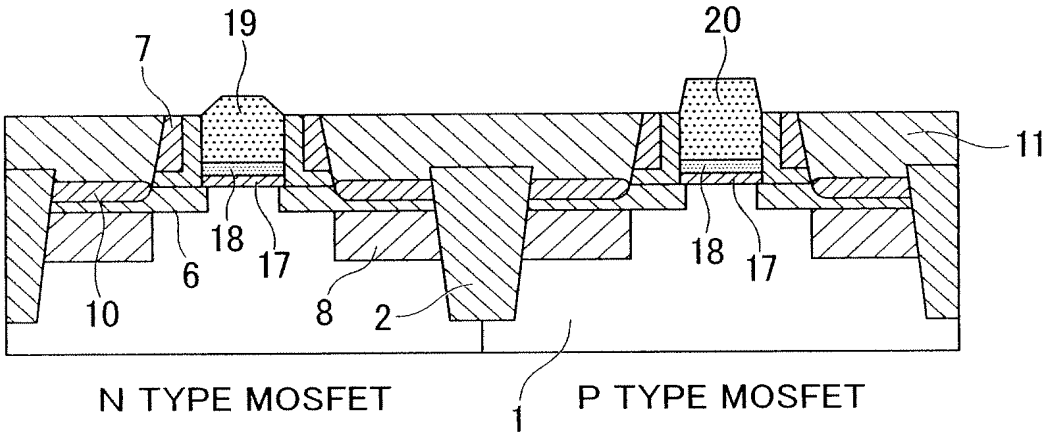


FIG. 2A

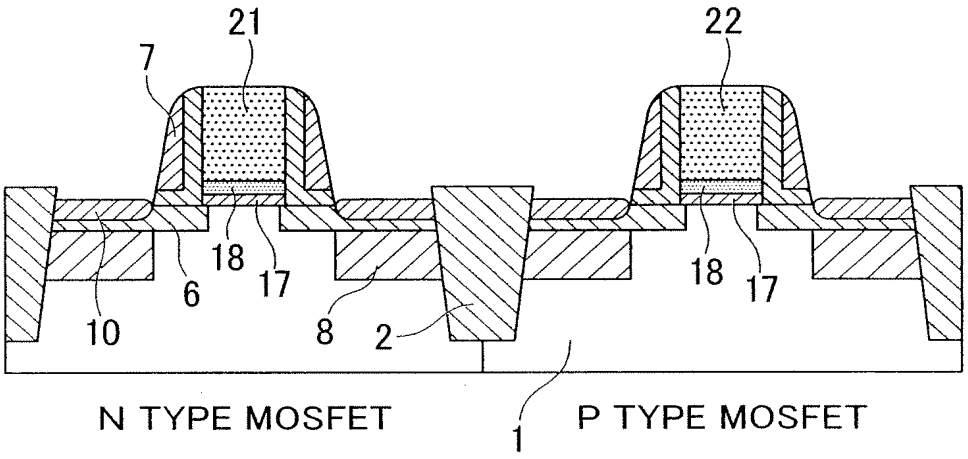


FIG. 2B

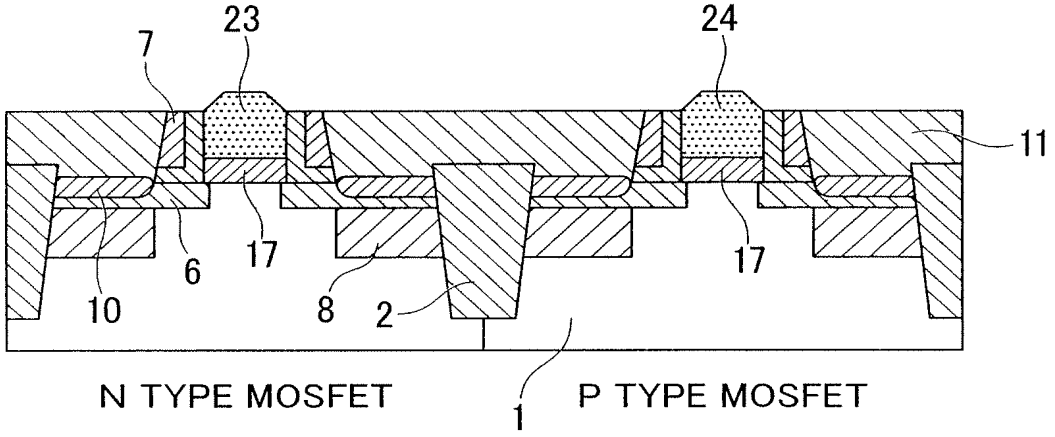


FIG. 2C

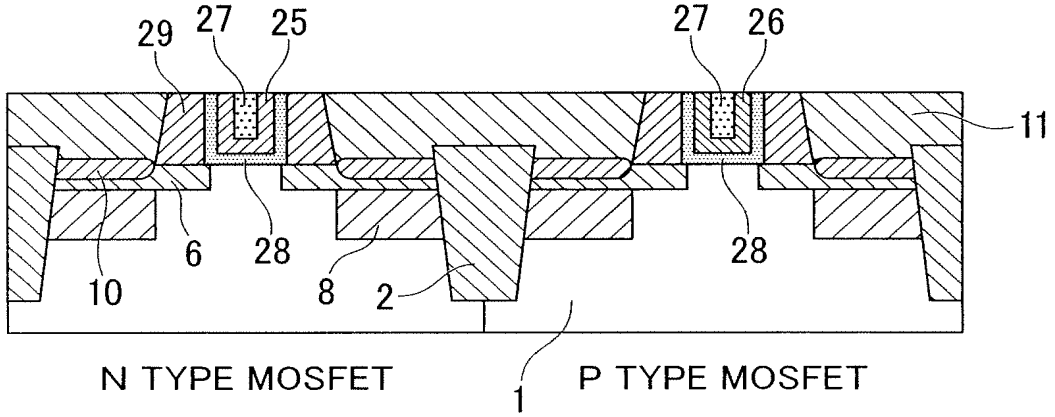


FIG. 3A

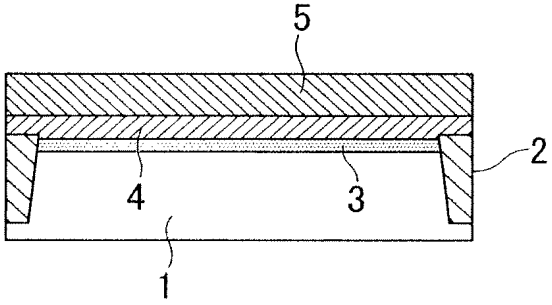


FIG. 3B

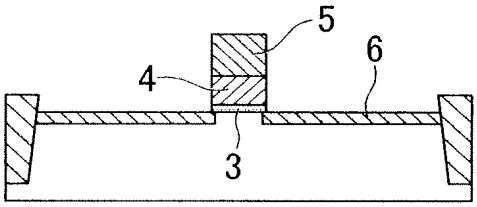


FIG. 3C

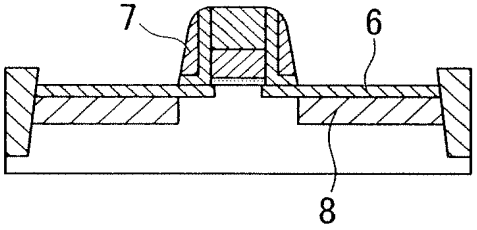


FIG. 3D

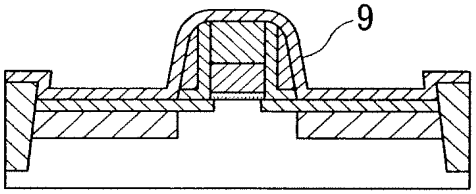


FIG. 3E

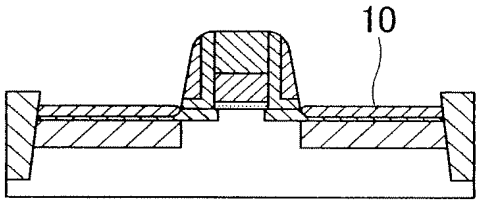


FIG. 3F

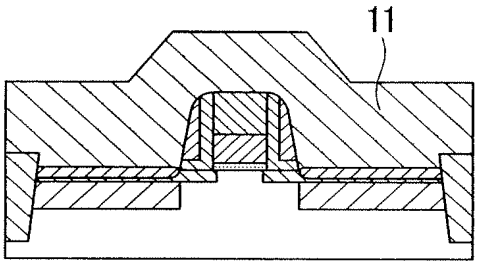


FIG. 3G

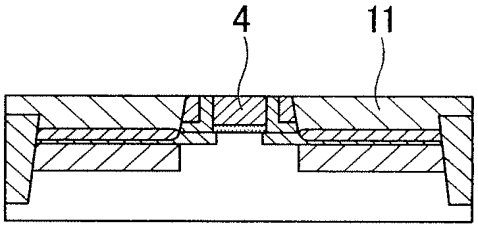


FIG. 4H

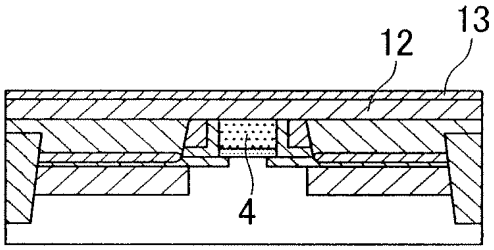


FIG. 4I

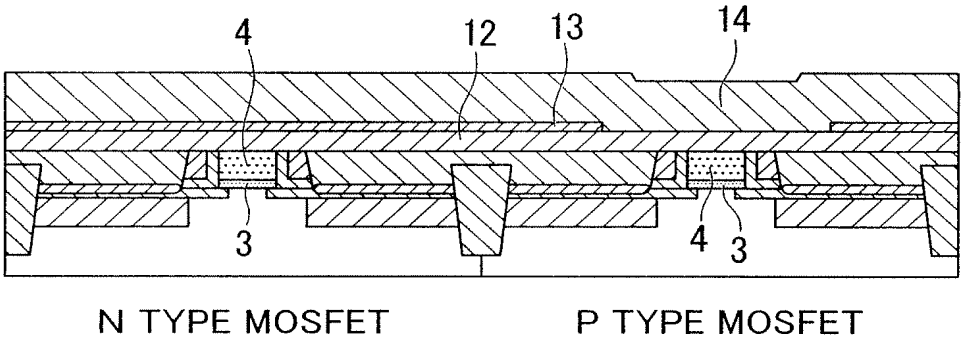


FIG. 4J

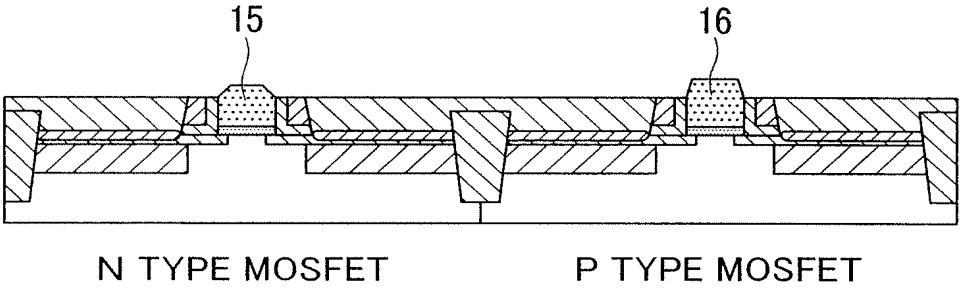


FIG. 5

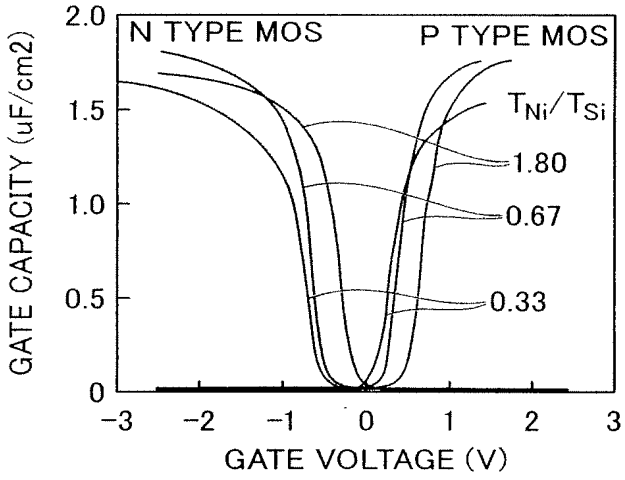

2.0
1.5
1.0
0.5
0
N TYPE MOS
P TYPE MOS
T_{Ni}/T_{Si}
1.80
0.67
0.33
GATE CAPACITY (uF/cm2)
−3
−2
−1
0
1
2
3
GATE VOLTAGE (V)

FIG. 6

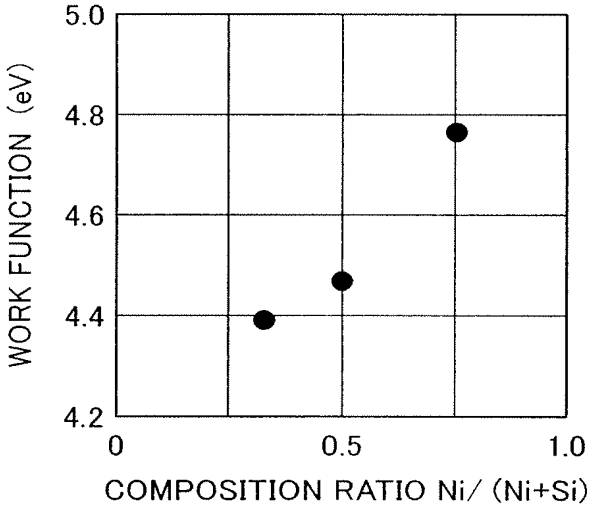

5.0
4.8
4.6
4.4
4.2
WORK FUNCTION (eV)
0
0.5
1.0
COMPOSITION RATIO Ni/ (Ni+Si)

FIG. 7

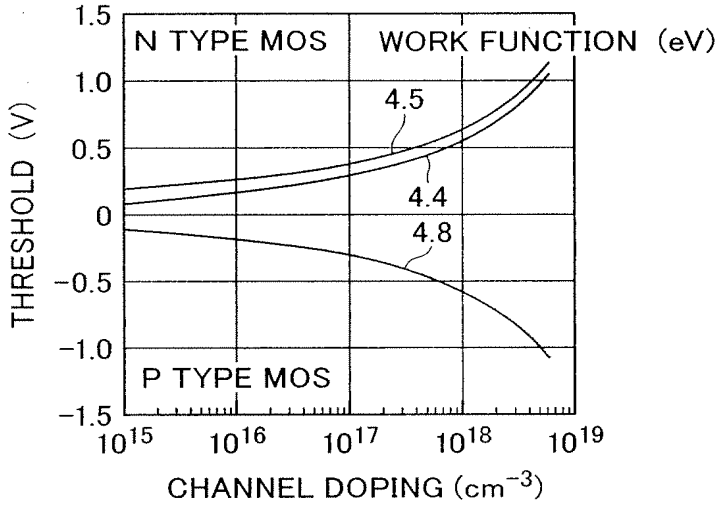

N TYPE MOS
WORK FUNCTION (eV)
4.5
4.4
4.8
P TYPE MOS
THRESHOLD (V)
1.5
1.0
0.5
0
−0.5
−1.0
−1.5
10^{15}
10^{16}
10^{17}
10^{18}
10^{19}
CHANNEL DOPING (cm^{-3})

FIG. 8

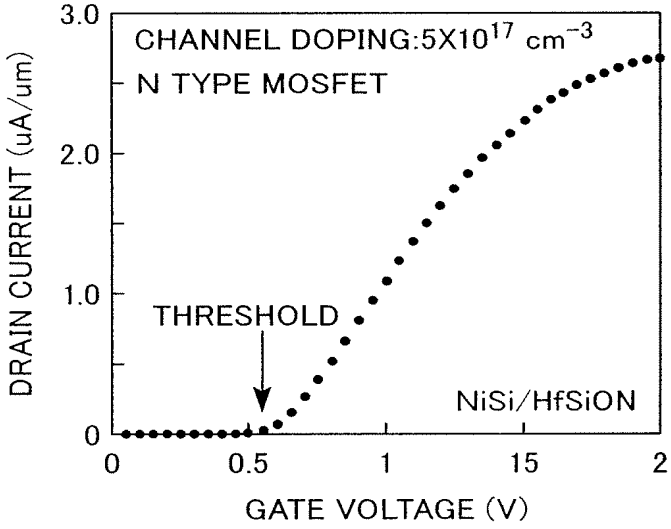

CHANNEL DOPING:5X10^{17} cm^{-3}
N TYPE MOSFET
THRESHOLD
NiSi/HfSiON
DRAIN CURRENT (uA/um)
3.0
2.0
1.0
0
0
0.5
1
15
2
GATE VOLTAGE (V)

FIG. 9

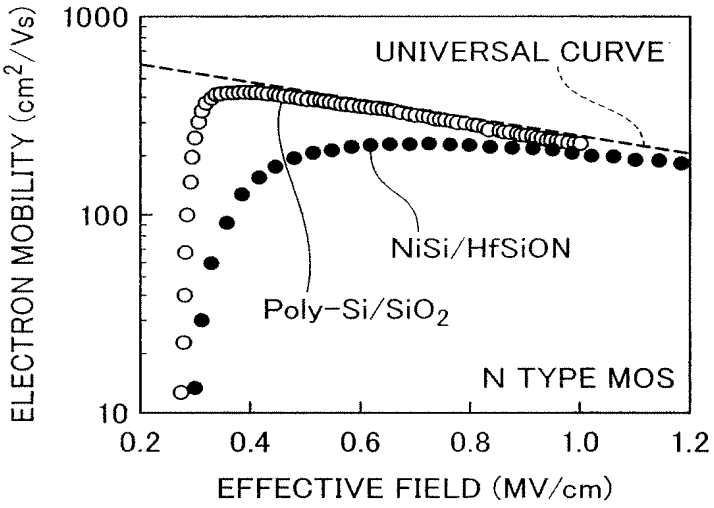

1000
100
10
ELECTRON MOBILITY (cm²/Vs)
UNIVERSAL CURVE
NiSi/HfSiON
Poly-Si/SiO2
N TYPE MOS
0.2
0.4
0.6
0.8
1.0
1.2
EFFECTIVE FIELD (MV/cm)

FIG. 10

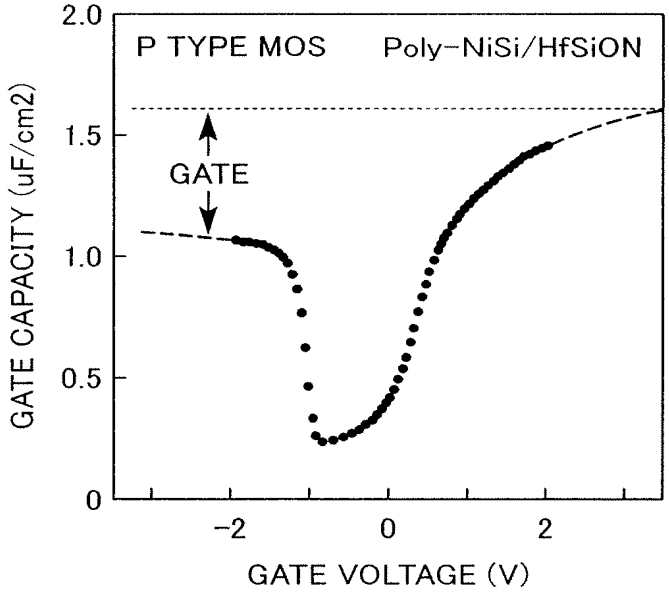

2.0
1.5
1.0
0.5
0
GATE CAPACITY (uF/cm2)
P TYPE MOS
Poly-NiSi/HfSiON
GATE
-2
0
2
GATE VOLTAGE (V)

FIG. 11

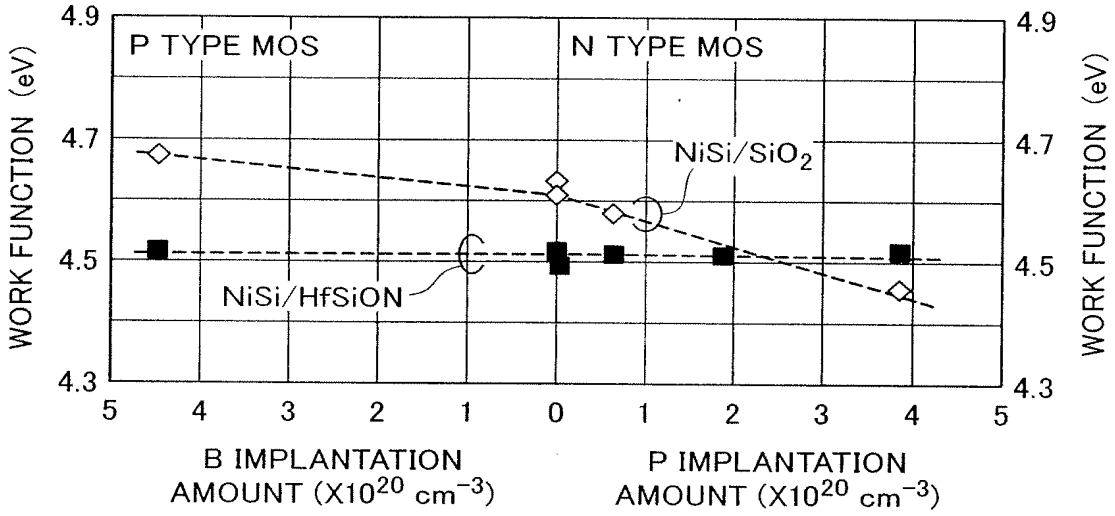
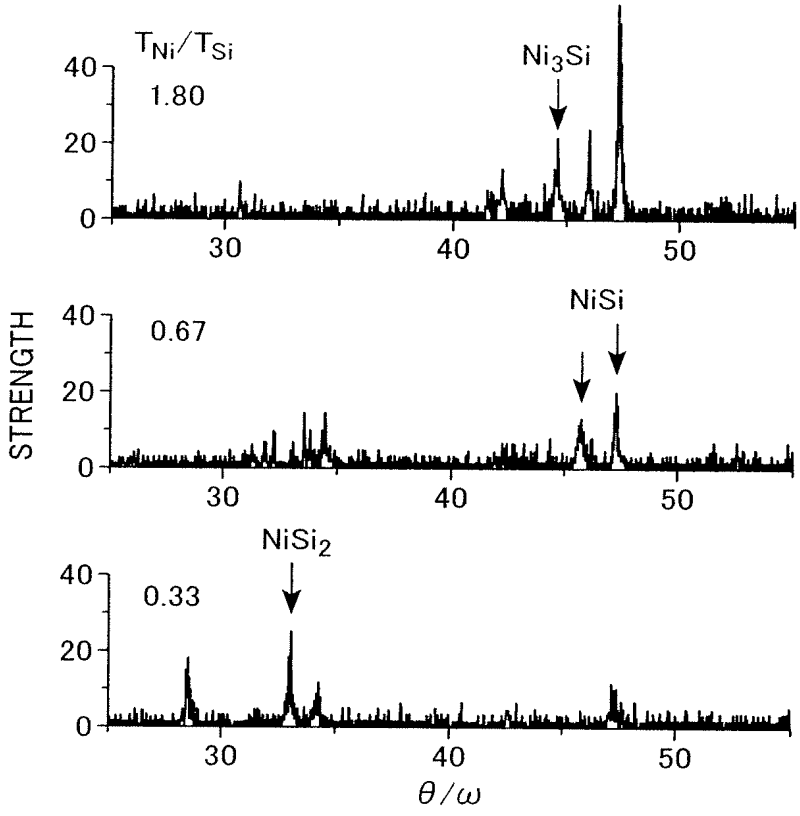

P TYPE MOS
N TYPE MOS
NiSi/SiO2
NiSi/HfSiON
WORK FUNCTION (eV)
4.9
4.7
4.5
4.3
5 4 3 2 1 0 1 2 3 4 5
B IMPLANTATION AMOUNT (X10^20 cm^-3)
P IMPLANTATION AMOUNT (X10^20 cm^-3)

FIG. 12


TNi/TSi
1.80
Ni3Si
0.67
NiSi
NiSi2
0.33
STRENGTH
40
20
0
30
40
50
θ/ω